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Architecture of Networks-on-Chip and Design Techniques

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Abstract: *As the quantity of VLSI design broaden, more processors or cores can be set on a single chip. Hence, the design of a Multi-Processor System-on-Chip (MP-SoC) architecture, which requests high throughput, low latency, and reliable global communication services, is impossible by simply utilizing current bus-based on-chip communication infrastructures. Networks-on-Chip (NoC) has been recommended as of late as a promising solution of on-chip interconnection network to provide better scalability, performance, and modularity for present and future MP-SoC architectures. Considering biological organisms have best adaptability than computer systems in handling with environmental changes or noise. A case study on the design of an evolvable neuromolecular hardware inspired from some biological evidence, which integrates inter- and intra-neuronal information processing, is illustrated in "A hardware design of neuromolecular network with enhanced resolvability: a bio-inspired approach" paper*

As the quantity of VLSI design broaden, more processors or cores can be set on a single chip. Hence, the design of a Multi-Processor System-on-Chip (MP-SoC) architecture, which requests high throughput, low latency, and reliable global communication services, is impossible by simply utilizing current bus-based on-chip communication infrastructures. Networks-on-Chip (NoC) has been recommended as of late as a promising solution of on-chip interconnection network to provide better scalability, performance, and modularity for present and future MP-SoC architectures.

"Networks on chips: structure and design methodologies" paper describe several NoC architectures and explain the design issues of communication performance, power consumption, signal integrity, and system scalability in an NoC. Then, a new Bidirectional NoC (BiNoC) architecture with a dynamically self-reconfigurable bidirectional channel is outlined, which can break the performance bottleneck caused by bandwidth restriction in conventional NoCs. Since buffers in on-chip networks constitute a vital proportion of the power consumption and the area of interconnects, decreasing the buffer size is an vital problem. "A buffer sizing algorithm for network on chips with multiple voltage-frequency islands" paper presents a two-phase algorithm to size the switch buffers in NoC in considering the support of multiple-frequency islands.

"Self-calibrated energy-efficient and reliable channels for on-chip interconnection networks" paper tells the design of an energy-efficient and reliable channel for on-chip interconnection networks (OCINs) utilizing a self-calibrated voltage scaling method with self-corrected green (SCG) coding scheme.

Among all NoC components, links that connect the NoC routers are the most power-hungry components. "Intelligent on/off dynamic link management for onchip networks" paper presents an intelligent dynamic power management policy for NoCs with enhanced predictive abilities depend on supervised online learning of the system status, where links are turned off and on via the use of a small and scalable neural network.

Monitoring and diagnostic systems are needed in modern NoC implementations to assure high performance and reliability. "Status data and communication aspects in dynamically clustered network-onchip monitoring," paper presents the design of a dynamically clustered NoC monitoring structure for traffic and fault monitoring is explained.

Considering biological organisms have best adaptability than computer systems in handling with environmental changes or noise. A case study on the design of an evolvable neuromolecular hardware inspired from some biological evidence, which integrates inter- and intra-neuronal information processing, is illustrated in "A hardware design of neuromolecular network with enhanced resolvability: a bio-inspired approach" paper